Remarks

Claims 13, 15 and 16 without prejudice have been amended. New claims 18-20 have been added. Therefore, claims 1-20 are now presented for examination.

In a Final Office Action mailed October 2, 2003, claims 1-2 stand rejected under 35 U.S.C. §102(b) as being anticipated by Collins et al. (U.S. Patent No. 6,507,818). Applicant submits that the present claims are patentable over Collins.

Collins discloses a system for integrating active and simulated decision making processes. The system includes a storage device 12 storing a representation of a domain model, a decision making module 14, a real-time system interface 16, a simulated event generator module 18, and an event processor module 20. The system 10 further comprises a simulation controller module 22, a simulation clock 24, a real-time clock 26, a resource domain status file 28, a simulated event file 30, and a real-time event file 32. See Collins at col. 3, ll. 66 – col. 4, ll. 13. The module 14 receives real-time domain events during the real-time mode of operation, and receives simulated domain events during the simulation mode (col. 5, ll. 40-45).

The event processor module 20 selects either the real-time mode or the simulation mode based on selections by system users. For example, system users can select the real-time mode to conduct active assignment and scheduling for technicians in the field. The simulation mode can be selected to evaluate the effects of potential changes to the resource domain model, to compare recommendations issued by module 14 with decisions made by system users, or to provide training for system users (col. 5, ll. 59-67).

Claim 1 recites:

A method comprising:
receiving real-time analog data at a personal computer implementing a general purpose operating system;
generating a real-time event at the personal computer indicating a request to process the real time data;
determining whether the real-time event has a higher priority than a first non-real time event being processed at the personal computer; and
processing the real-time data if the real-time event has a higher priority than the first non-real time event.

Applicant submits that nowhere in Collins is there disclosed receiving real-time analog data at a personal computer. Collins discloses receiving real-time and simulated events. Real-time events represent an actual change to a diverse object set, while a simulated event represents a simulated change to a diverse object set. However, there is no disclosure of the real-time events and simulated events being received as analog data. As a result, claim 1 is patentable over Collins.

Claims 2-6, 17 and 18 depend from claim 1 and include additional limitations. Therefore, claims 2-6 are also patentable over Collins.

Claim 7 recites:

A computer system comprising:
a chipset;
a bus coupled to the chipset; and
a central processing unit (CPU), coupled to the bus, to generate a real-time event upon receiving real-time analog data at the computer system and to process the real-time event if the real-time event has a higher priority than a non-real-time event.

Applicant submits that nowhere in Collins is there disclosed a CPU to generate a real-time event upon receiving real-time analog data at a computer system. Thus, for the reasons described above with respect to claim 1, claim 7 is also patentable over Collins. Because claims 8-12, 19 and 20 depend from claim 7 and include additional limitations, claims 8-12, 19 and 20 are also patentable over Collins.

Claim 13 recites:

> A central processing unit (CPU) comprising:
> a timer to generate timing signals at predetermined time intervals;
> a register coupled to the event mechanism to store real-time data received at the CPU as analog data;
> an event mechanism coupled to the timer and the register to generate real time events in response to receiving the timing signals and determining that real-time data is stored within the register; and
> an event handler coupled to the event mechanism to process the real-time events received from the event mechanism upon determining the relative priority between the real-time events and non-real-time events

Thus, for the reasons described above with respect to claims 1 and 7, claim 13 is also patentable over Collins. In addition, claim 13 is patentable over Collins because Collins does not disclose an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register. Since claims 14-17 depend from claim 13 and include additional limitations, claims 14-17 are also patentable over Collins.

In the Final Office Action, claims 3-6 stand rejected 35 U.S.C. §103 as being unpatentable over Collins et al. (U.S. Patent No. 6,507,818) in view of Mays et al. (U.S. Patent No. 6,035,321). Applicant submits that the present claims are patentable over Collins even in view of Mays.

Mays discloses a kernel for enforcing a hierarchical invocation structure that prevents upcalls by executing kernel operations during each invocation of code unit of application by another code unit. Kernel operations determine the priority of the invoking unit of code based on the hierarchy of the invocation structure. Only invocations by either lower priority units, or the unit itself are allowed. Once invoked, the kernel operates to establish a priority for the invoked task. The kernel provides various event mechanisms to provide for priority based preemption concurrently with the enforced invocation structure, thus allowing the handling of asynchronous events in a

multitasking environment. The event mechanisms allow a unit of code to signal the occurrence of a condition, which may be captured by other code units. The kernel determines the proper code unit for responding to the condition, and employs scope rules to further define the handling operation. Scheduling and tasking mechanisms schedule the handling of the condition and dispatch the handling of the event on a prioritized basis. See Mays at Abstract.

Nevertheless, Mays does not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving real-time analog data at a computer system, or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register. As discussed above, Collins does not disclose or suggest such a limitation. Thus, any combination of Collins and Mays would also not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving real-time analog data at a computer system, or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register. Consequently, the present claims are patentable over Collins in view of Mays.

In the Final Office Action, claims 13-15 stand rejected 35 U.S.C. §103 as being unpatentable over Collins et al. (U.S. Patent No. 6,507,818) in view of Mays et al. (U.S. Patent No. 6,035,321) and further in view of Matsui et al. (U.S. Patent No. 5,774,701). Applicant submits that the present claims are patentable over Collins and Mays even in view of Matsui.

Matsui discloses a microprocessor that operates at high and low clock frequencies. See Matsui at col. 2, ll. 23-30. However, Matsui does not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving real-time

analog data at a computer system or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register.

As discussed above, Collins and Mays do not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving real-time analog data at a computer system, or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register. Thus, any combination of Collins, Mays and Matsui would also not disclose or such limitations. Accordingly, the present claims are patentable over Collins in view of Mays, and further in view of Matsui.

In the Final Office Action, claims 7-12, 16 and 17 stand rejected 35 U.S.C. §103 as being unpatentable over Collins et al. (U.S. Patent No. 6,507,818) in view of Mays et al. (U.S. Patent No. 6,035,321), further in view of Matsui et al. (U.S. Patent No. 5,774,701) and further in view of Raamot (U.S. Patent No. 3,877,021). Applicant submits that the present claims are patentable over Collins, Mays and Matsui even in view of Raamot.

Raamot discloses a digital-to-analog converter having a high degree of resolution. See Raamot at Abstract. However, Raamot does not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving real-time analog data at a computer system, or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register.

As discussed above, neither Collins, Mays nor Matsui disclose or suggest such limitations. Thus, any combination of Collins, Mays, Matsui and Raamot would also not disclose or suggest receiving real-time analog data at a personal computer implementing a general purpose operating system, a CPU to generate a real-time event upon receiving

real-time analog data at a computer system, or an event mechanism to generate real time events in response to receiving timing signals and determining that real-time data is stored within a register. Accordingly, the present claims are patentable over Collins in view of Mays, further in view of Matsui and further in view of Raamot.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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